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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,419	02/12/2004	Christopher H. Dick	X-1505 US	4321

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EXAMINER	
PIERRE LOUIS, ANDRE	
ART UNIT	**PAPER NUMBER**
2123	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/777,419	DICK ET AL.	
	Examiner	Art Unit	
	Andre Pierre-Louis	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-24 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-24 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 12 February 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 have been presented for examination.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." State Street, 149 F.3d at 1373, 47USPQ2d at 1601-02. The purpose of this requirement is to limit patent protection to inventions that possess a certain level of "real world" value, as opposed to subject matter that represents nothing more than an idea or concept, or is simply a starting point for future investigation or research (Brenner v. Manson, 383 U.S. 519, 528-36, 148 USPQ 689, 693-96); In re Ziegler, 992, F.2d 1197, 1200-03, 26 USPQ2d 1600, 1603-06 (Fed. Cir. 1993)). Accordingly, a complete disclosure should contain some indication of the practical application for the claimed invention, i.e., why the applicant believes the claimed invention is useful. However, the mere fact that the claim may satisfy the utility requirement of 35 U.S.C. 101 does not mean that a useful result is achieved under the practical application requirement. The claimed invention as a whole must produce a "useful, concrete and tangible" result to have a practical application.

2.0 Claims 1-34 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims do not produce a useful, concrete, and tangible result. While transferring data values between from block to another, the claims as set forth do not provide the usefulness of having such data values transferred from one bock to another block. ***See MPEP 2106 [R2]***

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3.0 Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. Patent No.6, 389,379), in view of Cooke et al. (U.S. Patent No. 6,968,514).

3.1 In considering the independent claims 1, 23, Lin et al. substantially teaches a method for transferring data between blocks in a design during simulation, in particular the steps of: co-simulating a first hardware-implemented block on a hardware co-simulation platform, wherein the first hardware implemented block implements a first high-level block in the design simulated in a high-level modeling system (HLMS) (*fig.3, 67, col.27 line 45-col.28 line 57*); and transferring a first vector of data values received by the first high-level block to the first hardware-implemented block via a single call to a first function provided by an interface that

couples the HLMS to the first hardware implemented block (*fig.3,67, col.28 lines 34-57, col.46 lines 21-27*). Although Lin does not clear state that the transfer is done via a single call, he teaches transferring data from one block to another via a host computing processing system via PCI to an FPGA (*col.66 line 54-col.67 line 57*). Nevertheless, Cooke et al. substantially teaches a Block Based Design Methodology, which the transferring of data between multiple block of the design (*see col.35 lines 32-49*) and further teaches a burst data transferring using a bridge (*col.42 lines 55-63*). Lin et al. and Cooke et al. are analogous art because they are from the field of endeavor and that the method teaches by Cooke et al. is similar to that of Lin et al. Therefore, it would have been obvious to one ordinary skilled in the art at the time of the applicant's invention to combine the simulation method of Cooke et al. with the co-verification system and method of Lin et al. because Cooke et al. teaches the advantage of using a method that provides a methodology for constructing re-usable circuit blocks which takes account of the special requirements of programmable components, and facilitates the integration of such programmable components with non-programmable components (*col.5 lines 32-48*).

3.2 With regards to claims 2 and 14, the combined teachings of Lin et al. and Cooke et al. substantially teach the step of simulating operation of a second high-level block in the design (*see Lin et al. fig.3-5, 67, col.124 lines 25-52); and* transferring the first vector of data values from the second high-level block to the first high-level block (*see Lin et al. fig.3, 67, col.28 lines 34-57, col.46 lines 21-27; also see Cooke et al. col.35 lines 32-49 & col.42 lines 55-63).*

3.3 As per claims 3 and 15, the combined teachings of Lin et al. and Cooke et al. substantially teach the step of co-simulating a second hardware-implemented block on a

hardware co-simulation platform, wherein the second hardware, implemented block implements a second high-level block in the design simulated in the HLMS (*see Lin et al. fig.3, 67, col.27 line 45-col.28 line 57*); and transferring the first vector of data values from the second high-level block to the first high-level block (*see Lin et al. fig.3, 67, col.28 lines 34-57, col.46 lines 21-27; also see Cooke et al. col.35 lines 32-49 & col.42 lines 55-63*).

3.4 Regarding claim 4, the combined teachings of Lin et al. and Cooke et al. substantially teach the step of transferring a second vector of data values received by the interface from the first hardware-implemented block, to the first high-level block in response to a single call to a second function provided by the interface and invoked by the first high-level block (*fig.3, 67, col.28 lines 34-57, col.46 lines 21-27; also see Cooke et al. col.35 lines 32-49 & col.42 lines 55-63*).

3.5 With regards to claim 5, the combined teachings of Lin et al. and Cooke et al. substantially teach the step of simulating operation of a second high-level block in the design in the HLMS (*see Lin et al. fig.3-5, 67, col.124 lines 25-52*); and transferring the second vector of data values from the first high-level block to the second high-level block *(see Lin et al. fig.3, 67, col.28 lines 34-57, col.46 lines 21-27; also see Cooke et al. col.35 lines 32-49 & col.42 lines 55-63)*.

3.6 As per claim 6, the combined teachings of Lin et al. and Cooke et al. substantially teach the step of co-simulating a second hardware-implemented block on a hardware co-simulation platform, wherein the second hardware implemented block implements a second high-level block in the design simulated in the HLMS (*see Lin et al. fig.3, 67, col.27 line 45-col.28 line 57*); and transferring the second vector of data values from the first high-level block

to the second high-level block (*see Lin et al. fig.3, 67, col.28 lines 34-57, col.46 lines 21-27; also see Cooke et al. col.35 lines 32-49 & col.42 lines 55-63).*

3.7 Regarding claim 7 and 18, the combined teachings of Lin et al. and Cooke et al. substantially teach the step of that wherein the hardware co-simulation platform includes a field programmable gate array (FPGA), *see Lin et al. fig.1 (20) & fig.3 (250*), and the method further comprises: determining from the design a required size for a buffer used in transferring a frame of data *(see Cooke et al. col.41 line 5-col.42 line 63)*; establishing at least one buffer of the required size of the FPGA (*see Cooke et al. col.35 lines 32-49)*; and temporarily storing at least one of a first frame and a second frame in the buffer (see Cooke et al. *col.42 lines 55-63*).

3.8 As per claim 8, the combined teachings of Lin et al. and Cooke et al. substantially teach that for each vector that drives an output port determining an associated size of the vector, wherein the required size of the buffer is equal to the size of the vector (*see Lin et al. 36 line 41-col.37 line 13; also see Cooke et al. col.35 lines 32-67*).

3.9 With regards to claims 9 and 19, the combined teachings of Lin et al. and Cooke et al. substantially teach the step of determining the required size as a function of a value of a user-provided configuration parameter (*see Cooke et al. col.41 line 5-col.42 line 63).*

3.10 Regarding claims10 and 20, the combined teachings of Lin et al. and Cooke et al. substantially teach that the configuration parameter is associated a buffer-size compilation option of the HLMS *(see Lin et al. col.66 line 54-col.67 line 57; also see Cooke et al. col.53 line 20-col.54 line 42).*

3.11 As per claims 11 and 21, the combined teachings of Lin et al. and Cooke et al. substantially teach that one or more input/output ports each has an associated configuration

parameter value *(see Lin et al. col.66 line 54-col.67 line 57; also see Cooke et al. col.53 line 20-col.54 line 42).*

3.12 With regards to claims 12 and 22, the combined teachings of Lin et al. and Cooke et al. substantially teach estimating FPGA resources available for buffers (*see Lin et al. col.35 line 50-col.37line 13; also see Cooke et al. col.41 line 5-col.42 line 63*); and selecting one or more buffer sizes as a function of the estimated available resources (*see Lin et al. col.35 line 50-col.37line 13; also see Cooke et al. col.41 line 5-col.42 line 63).*

3.13 Regarding claims 13 and 24, the combined teachings of Lin et al. and Cooke et al. substantially teach a method for transferring data between blocks in a design during simulation, comprising: co-simulating a first hardware-implemented block in the design on a hardware co-simulation platform, wherein the first hardware-implemented block implements a first high-level block in the design simulated in a high-level modeling system (HLMS) (*see Lin et al. fig.3, 67, col.27 line 45-col.28 line 57*); accumulating, by the first high-level block in response to a plurality of input scalar values, the plurality of scalar data values in a vector of data *(see Cooke et al. col.35 lines 32-67)*; and transferring the vector of data from the first high-level block to the hardware-implemented block via a single first transfer instruction to an interface that couples the HLMS to the first hardware-implemented block (*see Lin et al. fig.3, 67, col.28 lines 34-57, col.46 lines 21-27; also see Cooke et al. col.35 lines 32-49 & col.42 lines 55-63).*

3.14 As per claim 16, the combined teachings of Lin et al. and Cooke et al. substantially teach the step of simulating operation of a second high-level block in the design in a high-level modeling system (HLMS) (*see Lin et al. fig.3-5, 67, col.49 lines 18-51, col.124 lines 25-52)*; and outputting a sequence of scalar values from a vector of data received by the first

high-level block from the first hardware-implemented block to the second high-level block (*see Lin et al. fig.3, 67, col.28 lines 34-57; also see Cooke et al. col.35 lines 32-49 & col.42 lines 55-63)*.

3.15 Regarding claim 17, the combined teachings of Lin et al. and Cooke et al. substantially teach the step of co-simulating a second hardware-implemented block on a hardware co-simulation platform, wherein the second hardware implemented block implements a second high-level block in the design (*see Lin et al. fig.3, 67, col.27 line 45-col.28 line 57*); and outputting a sequence of scalar values from a vector of data received by the first high-level block to the second high-level block (*see Lin et al. fig.3, 67, col.28 lines 34-57; also see Cooke et al. col.35 lines 32-49 & col.42 lines 55-63)*.

4.0 Claims 1,13,23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seungjun Lee (A Hardware-Software co-Simulation Environment, PHD Thesis University of California, Berkeley 1993), in view of Cooke et al. (U.S. Patent No. 6,968,514).

4.1 Regarding claims 1, 13,23-24, Lee substantially teaches a method for transferring data between blocks in a design during simulation, comprising: co-simulating a first hardware-implemented block in the design on a hardware co-simulation platform, wherein the first hardware-implemented block implements a first high-level block in the design simulated in a high-level modeling system (HLMS) (*see section 1.3 (1.3.4)*); accumulating, by the first high-level block in response to a plurality of input scalar values, the plurality of scalar data values in a vector of data *(see section 1.3)*; and transferring the vector of data from the first high-level block to the hardware-implemented block via a single first transfer instruction to an interface that couples the HLMS to the first hardware-implemented block (*see 1.3.4, 2.3.2, also*

see Ch. 5). Although Lee does not clearly state the term transferring the data via a single first transfer instruction, he teaches transferring data from one block to another *(see 1.3.4, ch.5).* Nevertheless, Cooke et al. substantially teaches a Block Based Design Methodology, which the transferring of data between multiple block of the design (*see col.35 lines 32-49*) and further teaches a burst data transferring using a bridge (*col.42 lines 55-63*), and further teaches accumulating data in a table form a matrix before transferring from one block to the other (*see col.35 lines 32-67.* Lee and Cooke et al. are analogous art because they are from the field of endeavor and that the method teaches by Cooke et al. is similar to that of Lee. Therefore, it would have been obvious to one ordinary skilled in the art at the time of the applicant's invention to combine the simulation method of Cooke et al. with the co-verification system and method of Lee because Cooke et al. teaches the advantage of using a method that provides a methodology for constructing re-usable circuit blocks which takes account of the special requirements of programmable components, and facilitates the integration of such programmable components with non-programmable components (*col.5 lines 32-48*).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5.1 Tabbara et al. (Fast Hardware-Software Co-Simulation Using VHDL Models, 12/4/1998).

6. Claims 1-24 are rejected and **this action is Non-Final**. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre Pierre-

Louis whose telephone number is 571-272-8636. The examiner can normally be reached on Mon-Fri, 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

March 14, 2007

APL

3/16/07

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